WHAT IS CLAIMED IS:

1. A magnetic memory device comprising:

a plurality of word lines and a plurality of dummy word lines arranged along a same direction;

a plurality of bit line pairs each formed with a first and second bit lines arranged in a direction perpendicular to the direction of said plurality of word lines and said plurality of dummy word lines;

a plurality of magnetic memory cells alternately arranged at intersections of said plurality of word lines and said first and second bit lines, and electrically connected with the corresponding first or second bit line in response to a selection of the corresponding word line;

a plurality of magnetic reference cells alternately arranged at intersections of said plurality of dummy word lines and said first and second bit lines, and electrically connected to the corresponding said first or second bit line in response to a selection of the corresponding dummy word line;

a data reading circuit performing a data reading based on a passing current of said first and second bit lines forming same said bit line pair; and

a row select unit controlling a selection of said plurality of word lines and said plurality of dummy word lines according to an address signal,

wherein said row select unit selects one of said plurality of word lines and one of said plurality of dummy word lines in a normal data reading such that said first and second bit lines forming each of said bit line pairs are connected to one of said plurality of magnetic memory cells and one of said plurality of magnetic reference cells, respectively, and sets each of said plurality of word lines to a non-select state and at the same time selects said plurality of dummy word lines in a first test mode such that said first and second bit lines forming each of said bit line pairs are connected to two of said plurality of magnetic reference cells, respectively.

2. The magnetic memory device according to claim 1, wherein each of said plurality of magnetic memory cells includes a first magneto-resistance element set to one of a high resistance state and a low resistance

state according to magnetically written-in data and a first access switch rendered conductive with a first resistance value as an on resistance in response to selection of said corresponding word line, said first magneto-resistance element and said first access switch being connected in series between said corresponding first or second bit line and a predetermined voltage,

each of said plurality of reference cells includes a second access switch and a second magneto-resistive element having a resistance similar to that of said first magneto-resistive element connected in series between said corresponding first or second bit line and the predetermined voltage, said second access switch being rendered conductive in response to a selection of said corresponding dummy word line,

said magnetic memory device further comprising a resistance control unit controlling an on resistance of said second access switch in a conductive state,

said resistance control unit controls the on resistance of said second access switch in the conductive state to a second resistance value for each of said plurality of magnetic reference cells in said normal data reading, and controls the on resistance of said second access switch to said second resistance value and a resistance value different from said second resistance value for one and the other of two of said magnetic reference cells connected to said first and second bit lines, respectively, in said first test mode, and

a sum of a resistance value of said second magneto-resistance element and said second resistance value is at an intermediate level of a sum of a resistance value of said each of first and second magneto-resistance element in said low resistance state and said first resistance value and a sum of a resistance value of each of said first and second magneto-resistance element in said high resistance state and said first resistance value.

3. The magnetic memory device according to claim 2, wherein said resistance control unit controls the on resistance of the second access switches in the conductive state to one and the other of said first and second resistance values respectively, in said two of said magnetic reference cells

connected to said first and second bit lines respectively in said first test mode.

4. The magnetic memory device according to claim 2, wherein said first access switch includes a first field effect transistor connected in series with said first magneto-resistance element between said corresponding first or second bit line and said predetermined voltage and having a gate connected to said corresponding word line,

said second access switch includes second and third field effect transistors connected in series with said second magneto-resistance element between said corresponding first or second bit line and said predetermined voltage,

said second field effect transistor has a gate connected to said corresponding dummy word line, and

said third field effect transistor has a gate receiving an input of reference voltage controlled by said resistance control unit.

5. The magnetic memory device according to claim 1, wherein

a cell resistance of each of said plurality of magnetic memory cells changes according to a level of magnetically written-in data,

each of said plurality of magnetic reference cells has a same configuration as each of said plurality of magnetic memory cells,

in each of said bit line pairs, to each of said magnetic reference cells connected to said first bit line and to each of said magnetic reference cells connected to said second bit line, said data are previously written in at complementary levels, respectively,

said magnetic memory device further comprises

a first switch for connecting each of said first bit lines to another said first bit line corresponding to other said bit line pair,

a second switch for connecting each of said second bit lines to another said second bit line corresponding to other said bit line pair, and

a switching control unit controlling on and off of said first and second switches, wherein

to said magnetic reference cells corresponding to two said first bit lines connectable with said first switch, said data are previously written in at complementary levels, respectively,

to said magnetic reference cells corresponding to two said second bit lines connectable with said second switch, said data are previously written in at complementary levels, respectively,

said switching control unit turns said first switch off and turns said second switch on when a selected memory cell is connected to said first bit line and turns said first switch on and turns said second switch off when said selected memory cell is connected to said second bit line in said normal data reading, and turns each of said first and second switches off in said first test mode.

6. The magnetic memory device according to claim 5, comprising

a plurality of spare word lines arranged along the same direction with the direction of said plurality of word lines and plurality of dummy word lines, and

a plurality of magnetic spare cells each having the same configuration as each of said plurality of magnetic memory cells, wherein

said plurality of magnetic spare cells are arranged alternately at intersections of said plurality of spare word lines and said first and second bit lines, and electrically connected to corresponding said first or second bit line in response to a selection of the corresponding spare word line,

said row select unit further controls a selection of said plurality of spare word lines and selects one of said plurality of spare word lines instead of the word line to be selected when the magnetic memory cell corresponding to the word line to be selected is defective in said normal data reading and selects one of said plurality of spare word lines instead of the dummy word line to be selected when the magnetic reference cell corresponding to said dummy word line to be selected is defective, and

when there is a defect in said plurality of reference cells, said data are previously written into said plurality of magnetic spare cells in a same manner with said plurality of reference cells.

7. The magnetic memory device according to claim 6, wherein said row select unit turns each of said plurality of word lines and said plurality of dummy word lines into a non-select state and selects said plurality of spare word lines such that said first and second bit lines forming each of said bit line pairs are connected to two of said plurality of magnetic spare cells in a second test mode.

8. The magnetic memory device according to claim 6, wherein

each of said plurality of magnetic memory cells includes a first magneto-resistance element having a resistance varied according to magnetically written in data and a first access switch rendered conductive in response to a selection of said corresponding word line, said magneto-resistance element and said first access switch being connected in series between said corresponding first or second bit line and a predetermined voltage,

each of said plurality of magnetic dummy cells includes a second access switch rendered conductive in response to a selection of said corresponding dummy word line and a second magneto-resistance element having a resistance similar to that of said first magneto-resistance element, said second access switch and said second magneto-resistance element being connected in series between said corresponding first or second bit line and the predetermined voltage and,

each of said plurality of magnetic spare cells includes a third access switch render conductive in response to a selection of said corresponding spare word line and a third magneto-resistance element having a resistance similar to that of said first magneto-resistance element, said third access switch and said third magneto-resistance element being connected in series between said corresponding first or second bit line and the predetermined voltage and, and

resistance values of said first, second and third access switches in a conductive state are substantially equal.

9. The magnetic memory device according to claim 1, further

comprising

a plurality of spare word lines arranged along the same direction with the direction of said plurality of word lines and said plurality of dummy word lines, and

a plurality of magnetic spare cells to be replaced with said plurality of magnetic reference cells, wherein

said plurality of magnetic spare cells are alternately arranged at intersections of said plurality of spare word lines and said first and second bit lines, and electrically connected to corresponding said first or second bit line in response to a selection of the corresponding spare word line, and

said row select unit further controls a selection of said plurality of spare word lines and turns each of said plurality of word lines and said plurality of dummy word lines to a non-select state and selects said plurality of spare word lines such that said first and second bit lines forming each of said bit line pairs are connected to two of said plurality of magnetic spare cells, respectively, in a second test mode.

10. The magnetic memory device according to claim 9, further comprising

a programming circuit including a programming element fixedly storing information in response to an external input and supplying a programming signal as an output corresponding to an existence of said external input to said programming element, wherein

said row select unit selects one of said plurality of spare word lines instead of the dummy word line to be selected when there is a defect in said magnetic reference cells, and

said row select unit determines whether there is a defect in said magnetic reference cells or not based on said programming signal in said normal data reading and based on an externally supplied electrical signal in a third test mode.